Effective and Adaptive Logic Design in VLSI for Digital Circuit Designing using Verilog

[1] Dr. S. Murali Mohan, [2] Mr. P. Prathap, [3]Mr. P. S. Rajakumar
[1]Professor, [2,3] Assistant Professor
[1, 2, 3]Mother Theresa Institute of Engineering and Technology, Palamaner, JNTUA University.

Abstract: In digital system design, the main constraint is minimum energy, compatibility, low power, etc. The main objective of the digital design is to achieve Minimum Energy Power system that can obtained by using adaptive logic. In digital circuits the logic used to implement effective designs is adaptive which is a very faster and technological advancement as innovative logic which is been used in almost every digital design to fulfil the major constraints. But additionally Nano sized magneticsystem and CMOS technology is been used to implement the adaptive logic in the digital circuit to extensively improve the efficiency of the energy. In order to achieve the minimum energy techniques the region will be having subsequent threshold and sub-threshold regionsand these both regions will be implemented in adaptive logic. Huge breakpoint of threshold region is in IoT device (Internet of Things) to reduce the power consumption or to increase the yield margins Timing-Error-Detection(TED) systems are been used. If there is conditional minimum voltage, if that is processed in the digital circuit then there will be a scope of occurring delay in the circuit. This delay is further improve as error in the circuit which will be over ridden by using canary circuit which is mainly used for error detection and error correction method, but this canary circuit extents its results in large delay in this regard toovercomethe disadvantage, adaptive logic circuit is been designed with a double gated latchcircuit in each stage of the circuit. This adaptive logic design circuit also undergoes some sought of delay in the circuit which can be over ridden by using a combination of XNOR gate and flip flop in the each section stage to stage for the verification of the signal error. Verilog Coding and implementation process developed by using XILINX ISE 14.3 Version tool.

Index Terms *- Canary circuit, Time margin, TEP (Timing Error Prevention), TED (Timing Error Detection).*

I. INTRODUCTION

Critical design requirement of every digital circuit is emerged as energy efficiency. Digital design concepts ensures the correct operation of every circuit, which is need to operate in low voltage by using scaling up concepts which resultant the voltage as low as possible. On constraints base and limitations based upon the potential of the circuit will be tested with voltage scaling up techniques which will result in correct operation of the circuit without producing any delay. If the digital circuit is operated with insufficient voltage range then there will a slow performance in the single circuit which will incur delay in the entire circuit [15]. Every design is designed in such a way that it will be operated in minimum energy consumption. Techniques like parallel processing and pipelining techniques proposed in order to reduce the signal delay in the circuit by operating the circuit at low voltage levels. Time margin technique is to overcome the above techniques.

II. BACK GROUND

In time margin technique the timing error probability variations are increased by implementing reduction methodologies. Variations are categorised in 2 namely spatial variation and temporal variation. Generally by the usage of spatial variation transistors are been effected and in this regard spatial variation is categorized as in two ways namely global variation and local variation. In this continuation global variation variables will be effecting the electrical characteristics of all the devices in the digital system. Due to randomness effect in the local variation which results in unpredictable in the characteristics in the transistor. Temporal variations are divided into states and temporal variation. State variation is effected during the fabrication period itself. Temporal variation is effected due to the cause of environmental changes, noise and aging of the components [1].In traditional design approach deals with the circuit delay which is caused by the scaling up voltage. In this context there are some high number of limitations for the traditional approach. These limitations can be overcome in two ways

1.By avoiding timing violation with the concept of predicting the occurrence of errors (Error prediction approach)

2. By correcting the errors(Error detection approach)[14].In this aspect there are popular methods for the error correctiontechniques:one among them which is more efficient and effectiveis thereplay and counter flow pipelining technique. Thesemethods are time consuming things, but one of the best methodfor the error correction with the delay in the digital circuit by propagating the cycle in the design pattern and covers all the stages in the system designed earlier. If the condition for theinstance ifthere are N cycles in a digital circuit it will have N pipeline stages. Some of the cycles failed due to some sought of delay incurred and those cycles are reissued with the token help of the clock signal in the system. The possibility for the entire system, takes 2N cycles and if any delay is occurred it will take 3N cycles at the end. The pipeline techniques are used to detect the errors and correct them based on conditions. In this concept if the error is generated in one particular stage that will be automatically corrected in that stage and thefollowing next cycle will be given to a new instruction cycle.

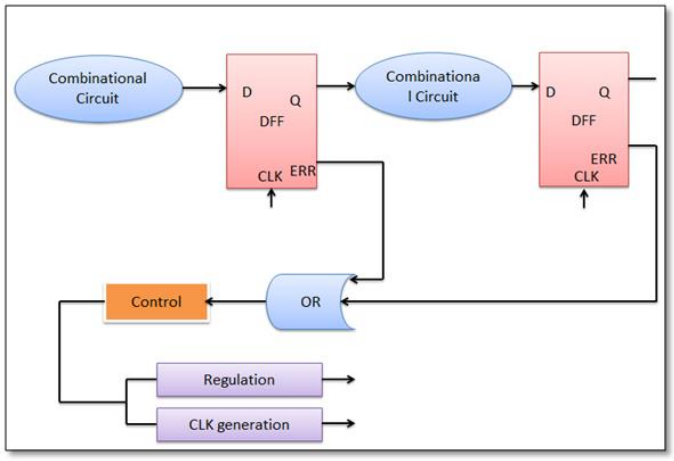

Fig. 1: Functional Representationof theTED system

III. TIMING ERROR DETECTIONSYSTEM (TED)

EDS is one of the major component of TED. If thepath gets failed in its way due to the generation of the digital error signals which is generated by EDS circuit, then this is approach called as synchronization [2]. This concept is generallyknown for the late signal detection conditions. EDS circuit is designed, if there is any chance of occurring ofany error those will be detected and using sequential and combinational circuit, got place in one critical logic circuit which will significantly reduce the delay in the circuit [13]. Timing error circuit signals are flagged OFF in the EDS circuit then the data will be transmitted to the digital logic circuit by using EXOR gate. This is used in every circuit to reduce the conditional and propagation delays. The output of combinational and sequential circuit signals given as the input to the EXOR gate circuit to in order to reduce the delay. At the end scenarios by using EDS circuit we reduced the delay for the combinational logic circuit.

IV. TIMING ERROR PREVENTION (TEP)

The TEP logic is formed by combining both TED and TB circuit. By combining both TED and TB which will generate a separate system which can tolerate the system performance the system performance may be effected by the late coming signals but by using TEP circuit the delay will be reduced in the system which even doesn't require any additional components which will use time margin technique. TB will be occurs normally when the delay signal is received, With EDS latch TB events will be detected. TB is nothing but Time Borrowing which will borrow the time from the previous stages when there is any delay signal and TB will be working as a latch [3]. This Latch will be having the enable and disable signals latch becomes transparent latch where the enable signal condition is high and the conditional processing speed will be remains high and more compared with the normal latch. TEP normallyoperates in generic transparent latch when the circuit enable signal is high i.e., '1' and the flow of work in normal latch when the circuit enable signal is low i.e., '0'. In TEP main concept is to borrow the time from other stages. These late signals are associated in both TED and TEP. When TEP is composed with 2 latches there is no need of any additional component in order to reduce the signal delay in the circuit. It is major advantage for TEP circuit compared to TED circuit.

V. SIMPLIFIED POWER MANAGEMENT FOR ADAPTIVE LOGIC

Generally some of the system which will be operated using battery in such systems Vbatt will be assigned to that battery which will be discharged after some usage of that battery so that automatically Vbatt will be decreased here VDD is kept constant so that battery discharged continuously[12]. Here very high significant amount of efficiency maintained in the digital circuit that ensures a fixed voltage in the circuit but due to that concept the battery is getting discharged. A large design is required to maintain the complex control circuit [4].Vref must be adjusted linearly with Vbatt in this regard to maintain the high range of efficiency over the large ranges for Vbatt. Here for the concept proof, we follows the theory that is in the circuit VDD to scale up which will change the Vbatt value based on condition, which will be constant for VDD/Vbatt ratio and then the resultant information is in zero fluctuations in the battery. This VDD/Vbatt ratio is called Voltage Conversion Ratio (VCR) of DC-DC converter. Generally Ideal VCR has no losses in the system the maximum conversion efficiency is defined in the terms of VCR and iVCR in the system.

$$nmax = VCR/iVCR = (m/n) * (VDD/Vbatt) \quad (1)$$

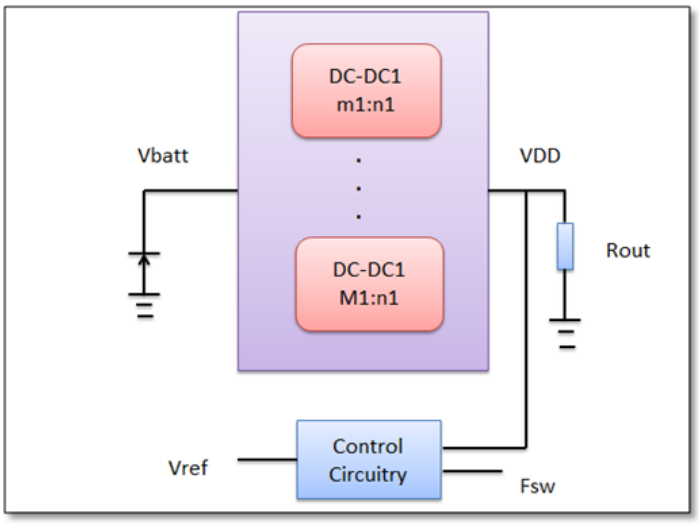

Fig.2 SC dc-dc converter

By changing Vbatt which enables 'nmax' to achieve wide range of Vbatt values. In this condition to provide the maximum efficiency across Vbatt novel technique has been implemented for scaling the known values as named as SIR technique. This is shortly abbreviated as Scaled Input Regulation technique [5]. This SIR technique is implemented for varying the voltage ranges in order to avoid constant voltage circulation among the entire digital circuit. This varying voltage is satisfied by both TEP and TED techniques [11]. These TEP and TED techniques re been used in adaptive logic concept. In order to maintain MEP VDD value is been scaled up or down accordingly to satisfy the constraints. To implement the traditional approach canary circuit is implemented.

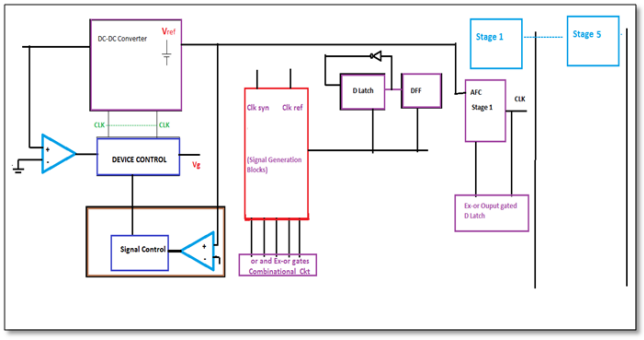

Fig 3. Adaptive logic circuit with multi stage connected to 16-bit ALU

VI. BASIC TRADITIONAL APPROACH

Time margin technique implemented to reduce the signal delay in the digital circuit, here it is called as canary circuit. There aretwo error correction circuits are designed namely canary circuit and razor circuit. These circuits will reduce the delay in the circuit [6]. Razor circuit is designed with a flip-flop in both main and shadow stage which is provided with clock in opposite polarity. The main operation of the shadow flip flop is to hold the correct values even though the main flip flop is delay with some particular signal. Error detection and error correction techniques are done using these flip flops [10]. At any instant of time shadow flip flop will be maintain the original values so in order to calculate the delay we will compare both the flip flops using EX-OR gate, If there is any difference between the flip flops EX-OR gate will be HIGH i.e., '1'. In this regard if any mismatchoccurred inboth the flip flops, then the multiplexer output automatically goes to high state as the output of the EX-OR gate is driven as the input to the multiplexer state. Razor flip flop will take the generated output of the shadow flip flop instead of borrowing it from the previous generated stages and corrected data will be sent to the followingnext stage. Razor circuit outputleads to a large design when several stages are inbuilt in the circuit [7]. Razor circuit has several drawbacks so canary circuit is been implemented to detect and correct the error in a single stage. At the final stage generated error is predicted by comparing both the flip flop and canary flip flop. Structured the data given to the canary flip flop and is delayed by the clock signal. Timing violations will be executed before the start function of the main flip flop.Advantages of canary circuit over razor circuit

1. Reduction in the signal delay
2. Timing errors functional protection
3. Variations measured

In this case to reduce the error in the circuit, without introducing any kind of delay in the system canary circuit is been implemented so that the delay will be reduced and this canary circuit will be connected to the digital circuit to improve the performance of the digital system. Canary circuit is modified by adding clock to that circuit so that the performance will be improved that modified circuit is nothing but the adaptive logic circuit.

VII. ADAPTIVE LOAD AND DICKSON CONVERTER

Main focus is to reduce delays and functional and signals errors in the circuit for this purpose the adaptive logic circuit has been designed based on the requirements. Here in this version canary circuit is regenerated with a dual latch and is placed at every stage at IN and OUT positions. Here to reduce the delay, we implemented varying voltageconcept instead of constant voltage technique i.e. Dickson DC-DC converter.In order to compensate the discharge battery concept [8]. For high efficiency SC Dickson converter is been implemented for the large load by using dual latch at every stage. If delay incurs in the circuit then time will be borrowed from other stages to compensate the time for the correct execution and that borrowed time will be recovered and this recovery will be managed by the clock control circuit.

In case of any flagged event TB the clock control circuit will latch up the signal at the initial phase of the next stage which will excludes the phase from the external clock. The discussed conditional structure will be possible only by combining the TB signals both TBE_NEG and TBE_POS. For avoiding the glitches the clock external will be gated in the middle phase by shifting clk_ref to 90 degrees.For the verification of the correct operation in every stage a combination circuit will be included in each stage which is nothing but a combination of X-OR gate and a flip flop. The prediction of errors in the circuit and correcting them is done by EDS circuit. Adaptive logic circuit is been designed in 5 stages for error detection and correction purpose.

VIII. RESULTS

The final step for the research shown with results, here the comparison between both the canary circuit delay and the adaptive logic circuit delay. The functional adaptive logic system is connected to the digital circuit using external clocks [9]. in order to compare the results the MAC unit taken as interfaced digital circuit. The Multiply-accumulate operation is used as a common step for computing the digital signal processing which will compute the product of two numbers and add the product to the accumulator. The hardware digital circuit used is Multiplier-Accumulator (MAC unit).

Structure	Delay
16-bit ALU	4.776ns
16-bit ALU connected to canary circuit	3.44ns
16-bit ALU connected to adaptive logic	2.414ns

Table 1. Comparison of the circuits

Here the simulation results invokes the delay comparison individual 8-bit MAC and 8-bit MAC connected to the adaptive logic circuit.

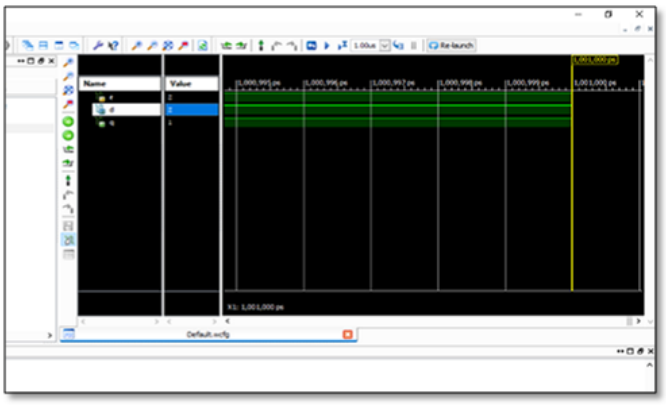

Fig 4: simulation result of D flip flop

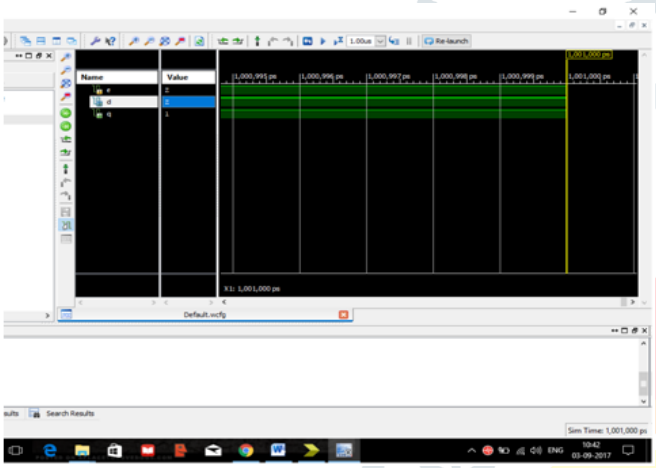

Fig 5: simulation result of D latch

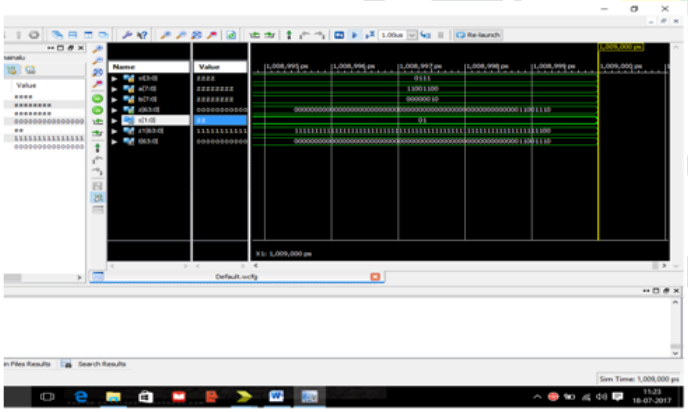

Fig 6: simulation result of EX-OR Gate

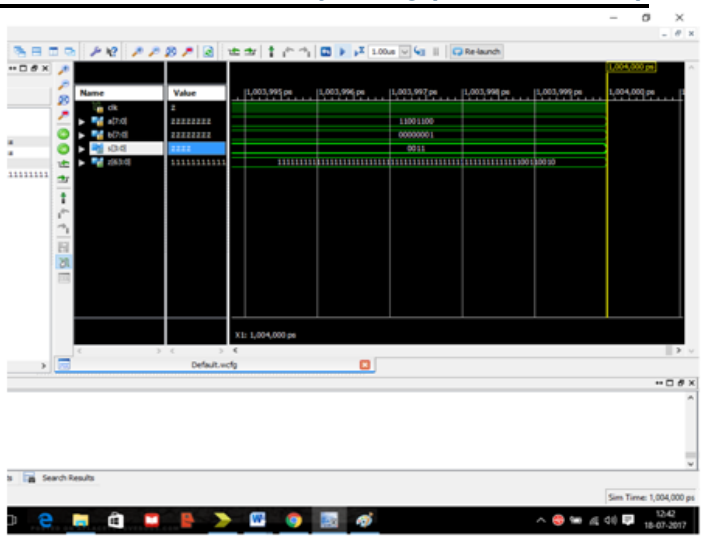

Fig 6: simulation result of 16-bit ALU connected to Adaptive circuit

IX.Conclusion

Supply voltage plays a main role in the digital circuit if the insufficient voltage is given to the digital circuit the output of that system will have delay, error and results in incorrect outputs. SC DC-DC converter is been used for the sufficient voltage in the digital circuit. In order to avoid the delay in the circuit canary circuit is been designed to reduce the error without including any stages in the digital system. Rather by using canary circuit the system performance is improved by using a dual latch in the circuit. When the circuit is composed with canary circuit, X-OR gate and a dual latch in each and every stage so that if there any delay occurs that can be verified by the additional circuit and reduced that will improve the performance of the digital system compared with the previous method.

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Author(s) Profile:

Dr. S. Murali Mohan, currently working as Professor at Mother Theresa Institute of Engineering and Technology, Palamaner, affiliated to JNTUA University in the Department of Electronics and Communication Engineering. He received his Doctorial Degree from S. V. University, Tirupathi, AP, He has published research papers in various international journals. His research interest areas are image processing, VLSI and neural networks.

Mr. P. Prathap is working as Assistant Professor, Mother Theresa Institute of Engineering and Technology, Palamaner, affiliated to JNTUA University in the Department of Electronics and Communication Engineering. He received his Bachelor's degree in ECE, 2008. He received his master's degree with the specialization of DSCE in the year 2010. He has published various national and international journals with the interest areas of Image Processing and Embedded Systems.

Mr. P. S. Raja Kumar is currently working as Assistant Professor at Mother Theresa Institute of Engineering and Technology, Palamaner, affiliated to JNTUA University in the Department of Electronics and Communication Engineering. He received his master's degree JNTUA, 2013 and Bachelor's degree in ECE 2009. He has published various international journals with the interest areas of VLSI and Image Processing.